CD54HC4046A, CD74HC4046A, CD54HCT4046A, CD74HCT4046A

Data sheet acquired from Harris Semiconductor
SCHS204J

February 1998 - Revised December 2003

High-Speed CMOS Logic Phase-Locked Loop with VCO

Features

- **Operating Frequency Range**
  - **Up to 18MHz (Typ) at V_{CC} = 5V**
  - **Minimum Center Frequency of 12MHz at V_{CC} = 4.5V**
- **Choice of Three Phase Comparators**
  - **EXCLUSIVE-OR**
  - **Edge-Triggered JK Flip-Flop**
  - **Edge-Triggered RS Flip-Flop**
- **Excellent VCO Frequency Linearity**
- **VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption**
- **Minimal Frequency Drift**
- **Operating Power Supply Voltage Range**
  - **VCO Section . . . . 3V to 6V**
  - **Digital Section . . . . 2V to 6V**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at VOL, VOH**

Applications

- **FM Modulation and Demodulation**
- **Frequency Synthesis and Multiplication**
- **Frequency Discrimination**
- **Tone Decoding**
- **Data Synchronization and Conditioning**
- **Voltage-to-Frequency Conversion**
- **Motor-Speed Control**

Description

The ’HC4046A and ’HCT4046A are high-speed silicon-gate CMOS devices that are pin compatible with the CD4046B of the “4000B” series. They are specified in compliance with JEDEC standard number 7.

The ’HC4046A and ’HCT4046A are phase-locked-loop circuits that contain a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

Ordering Information

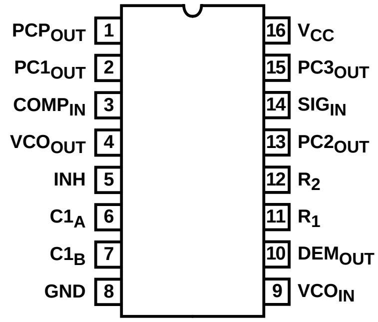
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4046AF3A	-55 to 125	16 Ld CERDIP
CD54HCT4046AF3A	-55 to 125	16 Ld CERDIP
CD74HC4046AE	-55 to 125	16 Ld PDIP
CD74HC4046AM	-55 to 125	16 Ld SOIC
CD74HC4046AMT	-55 to 125	16 Ld SOIC
CD74HC4046AM96	-55 to 125	16 Ld SOIC
CD74HC4046ANSR	-55 to 125	16 Ld SOP
CD74HC4046APWR	-55 to 125	16 Ld TSSOP
CD74HC4046APWT	-55 to 125	16 Ld TSSOP
CD74HCT4046AE	-55 to 125	16 Ld PDIP
CD74HCT4046AM	-55 to 125	16 Ld SOIC
CD74HCT4046AMT	-55 to 125	16 Ld SOIC
CD74HCT4046AM96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

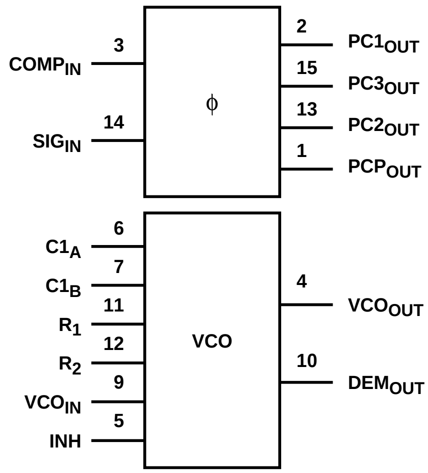
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Pinout

CD54HC4046A, CD54HCT4046A (CERDIP)
CD74HC4046A (PDIP, SOIC, SOP, TSSOP)
CD74HCT4046A (PDIP, SOIC)
TOP VIEW



Functional Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	Phase Comparator Pulse Output
2	$PC1_{OUT}$	Phase Comparator 1 Output
3	$COMP_{IN}$	Comparator Input
4	VCO_{OUT}	VCO Output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	GND	Ground (0V)
9	VCO_{IN}	VCO Input
10	DEM_{OUT}	Demodulator Output
11	R_1	Resistor R1 Connection
12	R_2	Resistor R2 Connection
13	$PC2_{OUT}$	Phase Comparator 2 Output
14	SIG_{IN}	Signal Input
15	$PC3_{OUT}$	Phase Comparator 3 Output
16	V_{CC}	Positive Supply Voltage

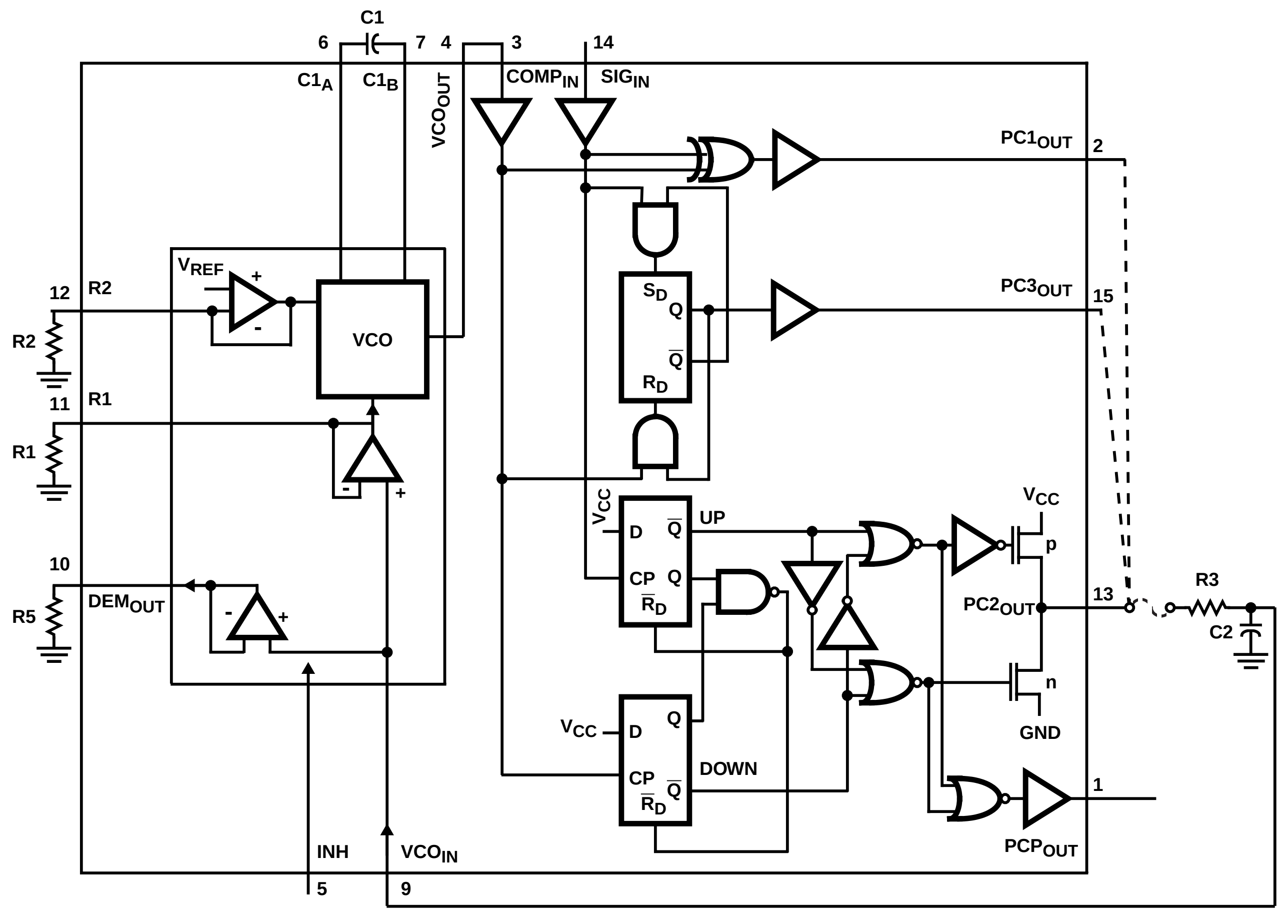


FIGURE 1. LOGIC DIAGRAM

General Description

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required. See logic diagram, Figure 1.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a specified duty factor of 50%. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

Phase Comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase Comparator 1 (PC1)

This is an Exclusive-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/\pi)\ (\phi SIG_{IN} - \phi COMP_{IN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Figure 2. The average of V_{DEM} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN}, and with this input the VCO oscillates at the center frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Figure 3.

The frequency capture range ($2f_C$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock behavior even with very noisy input signals. Typical of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO center frequency.

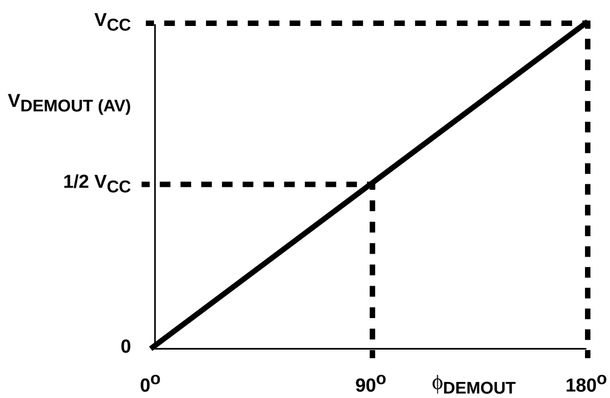


FIGURE 2. PHASE COMPARATOR 1: AVERAGE OUTPUT VOLTAGE vs INPUT PHASE DIFFERENCE: $V_{DEMOUT} = V_{PC1OUT} = (V_{CC}/\pi)\ (\phi SIG_{IN} - \phi COMP_{IN})$; $\phi_{DEMOUT} = (\phi SIG_{IN} - \phi COMP_{IN})$

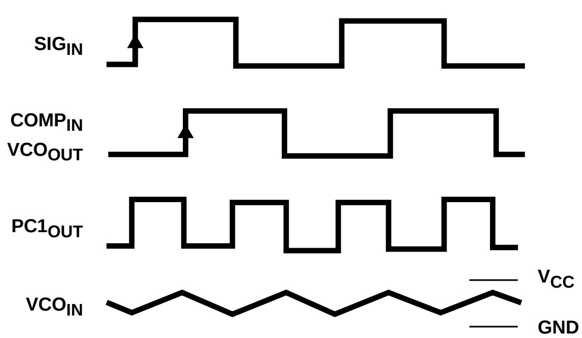


FIGURE 3. TYPICAL WAVEFORMS FOR PLL USING PHASE COMPARATOR 1, LOOP LOCKED AT f_o

Phase Comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a three-state output stage. The circuit functions as an up-down counter (Figure 1) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$V_{DEMOUT} = (V_{CC}/4\pi)\ (\phi SIG_{IN} - \phi COMP_{IN})$ where V_{DEMOUT} is the demodulator output at pin 10; $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The average output voltage from PC2, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Figure 4. Typical waveforms for the PC2 loop locked at f_o are shown in Figure 5.

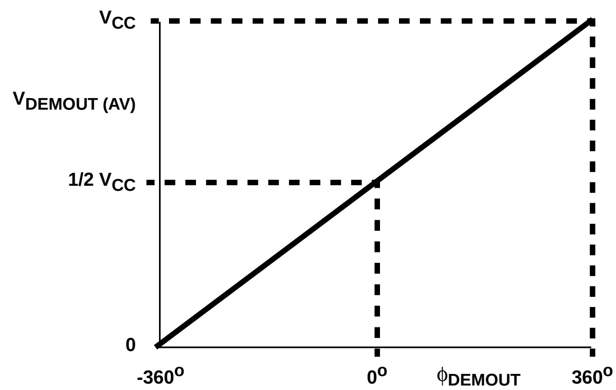


FIGURE 4. PHASE COMPARATOR 2: AVERAGE OUTPUT VOLTAGE vs INPUT PHASE DIFFERENCE: $V_{DEMOUT} = V_{PC2OUT}$ $= (V_{CC}/4\pi)\ (\phi SIG_{IN} - \phi COMP_{IN})$; $\phi_{DEMOUT} = (\phi SIG_{IN} - \phi COMP_{IN})$

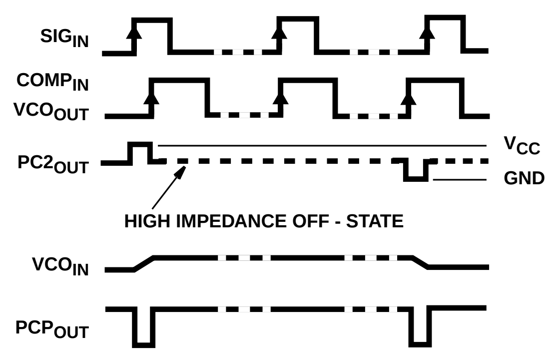


FIGURE 5. TYPICAL WAVEFORMS FOR PLL USING PHASE COMPARATOR 2, LOOP LOCKED AT f_o

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n- and p-type drivers are "OFF" (three-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and

frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in three-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p- and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN}, the VCO adjusts, via PC2, to its lowest frequency.

Phase Comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

V_{DEMOUT} = (V_{CC}/2p) (fSIG_{IN} - f$COMP_{IN}$) where V_{DEMOUT} is the demodulator output at pin 10; V_{DEMOUT} = V_{PC3OUT} (via low-pass filter).

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Figure 6. Typical waveforms for the PC3 loop locked at f_o are shown in Figure 7.

The phase-to-output response characteristic of PC3 (Figure 6) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the center frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as aconsequence the ripple content of the VCO input signal is higher. With no signal present at SIG_{IN}, the VCO adjusts, via PC3, to its highest frequency.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparator's sections are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and the HCT versions.

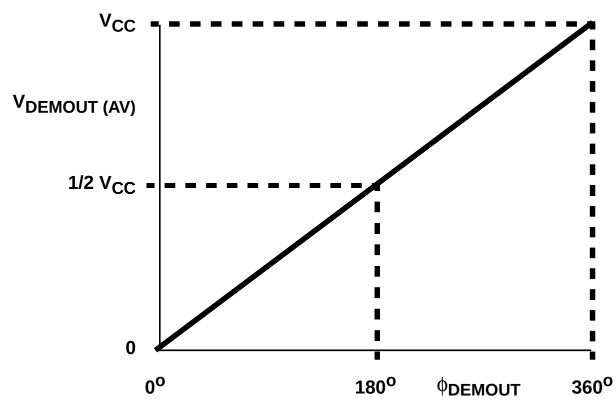


FIGURE 6. PHASE COMPARATOR 3: AVERAGE OUTPUT VOLTAGE vs INPUT PHASE DIFFERENCE: $V_{DEMOUT} = V_{PC3OUT} = (V_{CC}/2\pi)(\phi SIG_{IN} - \phi COMP_{IN})$; $\phi_{DEMOUT} = (\phi SIG_{IN} - \phi COMP_{IN})$

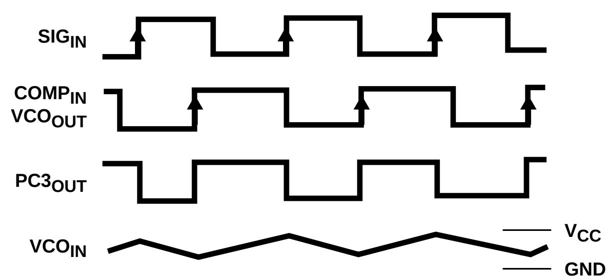


FIGURE 7. TYPICAL WAVEFORMS FOR PLL USING PHASE COMPARATOR 3, LOOP LOCKED AT f_o

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . .±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . .±25mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . .±25mA
DC V_{CC} or Ground Current, I_{CC} . . . .±50mA

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
E (PDIP) Package . . . . 67°C/W
M (SOIC) Package . . . . 73°C/W
NS (SOP) Package . . . . 64°C/W
PW (TSSOP) Package . . . . 108°C/W
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . .2V to 6V
HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
VCO SECTION												
INH High Level Input Voltage	V_{IH}	-	-	3	2.1	-	-	2.1	-	2.1	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
INH Low Level Input Voltage	V_{IL}	-	-	3	-	-	0.9	-	0.9	-	0.9	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
VCO_{OUT} High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	3	2.9	-	-	2.9	-	2.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
VCO_{OUT} High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
VCO_{OUT} Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
VCO_{OUT} Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
C1A, C1B Low Level Output Voltage (Test Purposes Only)	V_{OL}	V_{IL} or V_{IH}	4	4.5	-	-	0.40	-	0.47	-	0.54	V
			5.2	6	-	-	0.40	-	0.47	-	0.54	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
INH VCO_{IN} Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
R1 Range (Note 2)	-	-	-	4.5	3	-	300	-	-	-	-	kΩ
R2 Range (Note 2)	-	-	-	4.5	3	-	300	-	-	-	-	kΩ
C1 Capacitance Range	-	-	-	3	-	-	No Limit	-	-	-	-	pF
				4.5	-	-		-	-	-	-	pF
				6	-	-		-	-	-	-	pF
VCO_{IN} Operating Voltage Range	-	Over the range specified for R1 for Linearity See Figure 10, and 34 - 37 (Note 3)		3	1.1	-	1.9	-	-	-	-	V
				4.5	1.1	-	3.2	-	-	-	-	V
				6	1.1	-	4.6	-	-	-	-	V
PHASE COMPARATOR SECTION												
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
PCP_{OUT}, PCn OUT High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
				4.5	4.4	-	-	4.4	-	4.4	-	V
				6	5.9	-	-	5.9	-	5.9	-	V
PCP_{OUT}, PCn OUT High-Level Output Voltage TTL Loads	V_{OH}	V_{IL} or V_{IH}	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
PCP_{OUT}, PCn OUT Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
				4.5	-	-	0.1	-	0.1	-	0.1	V
				6	-	-	0.1	-	0.1	-	0.1	V
PCP_{OUT}, PCn OUT Low-Level Output Voltage TTL Loads	V_{OL}	V_{IL} or V_{IH}	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
SIG_{IN}, $COMP_{IN}$ Input Leakage Current	I_I	V_{CC} or GND	-	2	-	-	±3	-	±4	-	±5	µA
				3	-	-	±7	-	±9	-	±11	µA
				4.5	-	-	±18	-	±23	-	±29	µA
				6	-	-	±30	-	±38	-	±45	µA
$PC2_{OUT}$ Three-State Off-State Current	I_{OZ}	V_{IL} or V_{IH}	-	6	-	-	±0.5	-	±5	-	±10	µA
SIG_{IN}, $COMP_{IN}$ Input Resistance	R_I	V_I at Self-Bias Operation Point: ΔV_I = 0.5V, See Figure 10		3	-	800	-	-	-	-	-	kΩ
				4.5	-	250	-	-	-	-	-	kΩ
				6	-	150	-	-	-	-	-	kΩ
DEMODULATOR SECTION												
Resistor Range	R_S	at R_S > 300kΩ Leakage Current Can Influence V_{DEMOUT}		3	50	-	300	-	-	-	-	kΩ
				4.5	50	-	300	-	-	-	-	kΩ
				6	50	-	300	-	-	-	-	kΩ

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Offset Voltage VCO_{IN} to V_{DEM}	V_{OFF}	$V_I = V_{VCO\ IN} = \frac{V_{CC}}{2}$ Values Taken Over R_S Range See Figure 23		3	-	±30	-	-	-	-	-	mV
				4.5	-	±20	-	-	-	-	-	mV
				6	-	±10	-	-	-	-	-	mV
Dynamic Output Resistance at DEM_{OUT}	R_D	$V_{DEMOUT} = \frac{V_{CC}}{2}$		3	-	25	-	-	-	-	-	Ω
				4.5	-	25	-	-	-	-	-	Ω
				6	-	25	-	-	-	-	-	Ω
Quiescent Device Current	I_{CC}	Pins 3, 5 and 14 at V_{CC} Pin 9 at GND, I_1 at Pins 3 and 14 to be excluded		6	-	-	8	-	80	-	160	µA
HCT TYPES												
VCO SECTION												
INH High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
INH Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
VCO_{OUT} High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
VCO_{OUT} High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
VCO_{OUT} Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
VCO_{OUT} Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
C1A, C1B Low Level Output Voltage (Test Purposes Only)	V_{OL}	V_{IH} or V_{IL}	4	4.5	-	-	0.40	-	0.47	-	0.54	V
INH VCO_{IN} Input Leakage Current	I_I	Any Voltage Between V_{CC} and GND		5.5	-		±0.1	-	±1	-	±1	µA
R1 Range (Note 2)	-	-	-	4.5	3	-	300	-	-	-	-	kΩ
R2 Range (Note 2)	-	-	-	4.5	3	-	300	-	-	-	-	kΩ
C1 Capacitance Range	-	-	-	4.5	0	-	No Limit	-	-	-	-	pF
VCO_{IN} Operating Voltage Range	-	Over the range specified for R1 for Linearity See Figure 10, and 34 - 37 (Note 3)		4.5	1.1	-	3.2	-	-	-	-	V
PHASE COMPARATOR SECTION												
SIG_{IN}, $COMP_{IN}$ DC Coupled High-Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
SIG_{IN}, $COMP_{IN}$ DC Coupled Low-Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
PCP_{OUT}, PCn OUT High-Level Output Voltage CMOS Loads	V_{OH}	V_{IL} or V_{IH}	-	4.5	4.4	-	-	4.4	-	4.4	-	V
PCP_{OUT}, PCn OUT High-Level Output Voltage TTL Loads	V_{OH}	V_{IL} or V_{IH}	-	4.5	3.98	-	-	3.84	-	3.7	-	V
PCP_{OUT}, PCn OUT Low-Level Output Voltage CMOS Loads	V_{OL}	V_{IL} or V_{IH}	-	4.5	-	-	0.1	-	0.1	-	0.1	V
PCP_{OUT}, PCn OUT Low-Level Output Voltage TTL Loads	V_{OL}	V_{IL} or V_{IH}	-	4.5	-	-	0.26	-	0.33	-	0.4	V
SIG_{IN}, $COMP_{IN}$ Input Leakage Current	I_I	Any Voltage Between V_{CC} and GND	-	5.5	-	-	±30		±38		±45	µA
$PC2_{OUT}$ Three-State Off-State Current	I_{OZ}	V_{IL} or V_{IH}	-	5.5	-	-	±0.5	±5	-	-	±10	µA
SIG_{IN}, $COMP_{IN}$ Input Resistance	R_I	V_I at Self-Bias Operation Point: ΔV_I = 0.5V, See Figure 10		4.5	-	250	-	-	-	-	-	kΩ
DEMODULATOR SECTION												
Resistor Range	R_S	at R_S > 300kΩ Leakage Current Can Influence $V_{DEM\ OUT}$		4.5	5	-	300	-	-	-	-	kΩ
Offset Voltage VCO_{IN} to V_{DEM}	V_{OFF}	$V_I = V_{VCO\ IN} = \frac{V_{CC}}{2}$ Values taken over R_S Range See Figure 23		4.5	-	±20	-	-	-	-	-	mV
Dynamic Output Resistance at DEM_{OUT}	R_D	$V_{DEM\ OUT} = \frac{V_{CC}}{2}$		4.5	-	25	-	-	-	-	-	Ω
Quiescent Device Current	I_{CC}	V_{CC} or GND	-	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 4)	V_{CC} -2.1 Excluding Pin 5	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

2. The value for R1 and R2 in parallel should exceed 2.7kΩ.
3. The maximum operating voltage can be as high as V_{CC} -0.9V, however, this may result in an increased offset voltage.
4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
INH	1

NOTE: Unit load is ΔI_{CC} limit specific in DC Electrical Specifications Table, e.g., 360µA max. at 25°C.

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES											
PHASE COMPARATOR SECTION											
Propagation Delay SIG_{IN}, $COMP_{IN}$ to PCI_{OUT}	t_{PLH}, t_{PHL}		2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
			6	-	-	34	-	43	-	51	ns
SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}			2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
			6	-	-	51	-	64	-	77	ns
SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$			2	-	-	245	-	305	-	307	ns
			4.5	-	-	49	-	61	-	74	ns
			6	-	-	42	-	52	-	63	ns
Output Transition Time	t_{THL}, t_{TLH}		2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Enable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}, t_{PZL}		2	-	-	265	-	330	-	400	ns
			4.5	-	-	53	-	66	-	80	ns
			6	-	-	45	-	56	-	68	ns
Output Disable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PHZ}, t_{PLZ}		2	-	-	315	-	395	-	475	ns
			4.5	-	-	63	-	79	-	95	ns
			6	-	-	54	-	67	-	81	ns
AC Coupled Input Sensitivity (P-P) at SIG_{IN} or $COMP_{IN}$		$V_{I(P-P)}$	3	-	11	-	-	-	-	-	mV
			4.5	-	15	-	-	-	-	-	mV
			6	-	33	-	-	-	-	-	mV
VCO SECTION											
Frequency Stability with Temperature Change	$\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ, $R_2 = \infty$	3	-	0.11	-	-	-	-	-	%/°C
			4.5	-	0.11	-	-	-	-	-	%/°C
			6	-	0.11	-	-	-	-	-	%/°C
Maximum Frequency	f_{MAX}	C_1 = 50pF R_1 = 3.5kΩ $R_2 = \infty$	3	-	24	-	-	-	-	-	MHz
			4.5	-	24	-	-	-	-	-	MHz
			6	-	24	-	-	-	-	-	MHz
		C_1 = 0pF R_1 = 9.1kΩ $R_2 = \infty$	3	-	38	-	-	-	-	-	MHz
			4.5	-	38	-	-	-	-	-	MHz
			6	-	38	-	-	-	-	-	MHz

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Center Frequency		C_1 = 40pF, R_1 = 3kΩ, R_2 = ∞, VCO_{IN} = VCC/2	3	7	10	-	-	-	-	-	MHz
			4.5	12	17	-	-	-	-	-	MHz
			6	14	21	-	-	-	-	-	MHz
Frequency Linearity	Δf_{VCO}	R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF	3	-	0.4	-	-	-	-	-	%
			4.5	-	0.4	-	-	-	-	-	%
			6	-	0.4	-	-	-	-	-	%
Offset Frequency		R_2 = 220kΩ, C_1 = 1nF	3	-	400	-	-	-	-	-	kHz
			4.5	-	400	-	-	-	-	-	kHz
			6	-	400	-	-	-	-	-	kHz
DEMODULATOR SECTION											
V_{OUT} V_S f_{IN}		R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF, R_S = 10kΩ, R_3 = 100kΩ, C_2 = 100pF	3	-	-	-	-	-	-	-	mV/kHz
			4.5	-	330	-	-	-	-	-	mV/kHz
			6	-	-	-	-	-	-	-	mV/kHz
HCT TYPES											
PHASE COMPARATOR SECTION											
Propagation Delay SIG_{IN}, $COMP_{IN}$ to PCI_{OUT}	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	45	-	56	-	68	ns
SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	68	-	85	-	102	ns
SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	58	-	73	-	87	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Output Enable Time, SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$	t_{PZH}, t_{PZL}	C_L = 50pF	4.5	-	-	60	-	75	-	90	pF
Output Disable Time, SIG_{IN}, $COMP_{IN}$ to PCZ_{OUT}	t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	-	68	-	85	-	102	pF
AC Coupled Input Sensitivity ($_{P-P}$) at SIG_{IN} or $COMP_I$		$V_{I(P-P)}$	4.5	-	15	-	-	-	-	-	mV
VCO SECTION											
Frequency Stability with Temperature Change	$\frac{\Delta f}{\Delta T}$	R_1 = 100kΩ, R_2 = ∞	4.5	-	0.11	-	-	-	-	-	%/°C
Maximum Frequency	f_{MAX}	C_1 = 50pF, R_1 = 3.5kΩ, R_2 = ∞	4.5	-	24	-	-	-	-	-	MHz
		C_1 = 0pF, R_1 = 9.1kΩ, R_2 = ∞	4.5	-	38	-	-	-	-	-	MHz
Center Frequency		C_1 = 40pF, R_1 = 3kΩ, R_2 = ∞, VCO_{IN} = VCC/2	4.5	12	17	-	-	-	-	-	MHz
Frequency Linearity	Δf_{VCO}	R_1 = 100kΩ, R_2 = ∞, C_1 = 100pF	4.5	-	0.4	-	-	-	-	-	%

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Offset Frequency		R_2 = 220kΩ C_1 = 1nF	4.5	-	400	-	-	-	-	-	kHz
DEMODULATOR SECTION											
V_{OUT} V_S f_{IN}		R_1 = 100kΩ R_2 = ∞ C_1 = 100pF R_S = 10kΩ R_3 = 100kΩ C_2 = 100pF	4.5	-	330	-	-	-	-	-	mV/kHz

Test Circuits and Waveforms

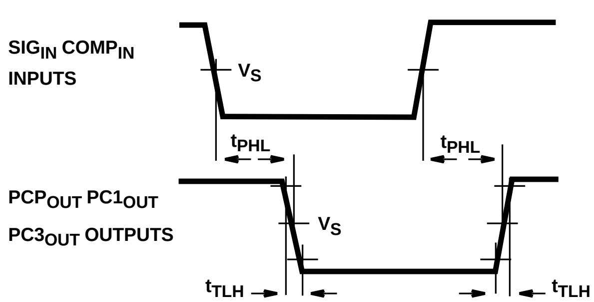


FIGURE 8. INPUT TO OUTPUT PROPAGATION DELAYS AND OUTPUT TRANSITION TIMES

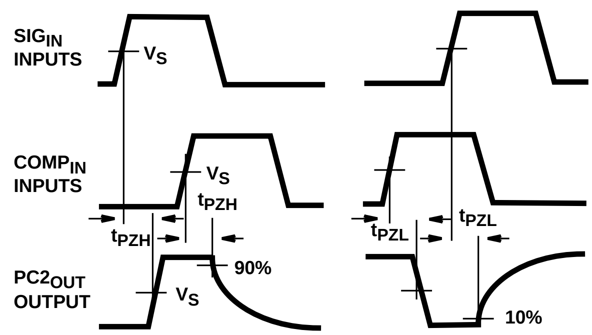


FIGURE 9. THREE STATE ENABLE AND DISABLE TIMES FOR $PC2_{OUT}$

Typical Performance Curves

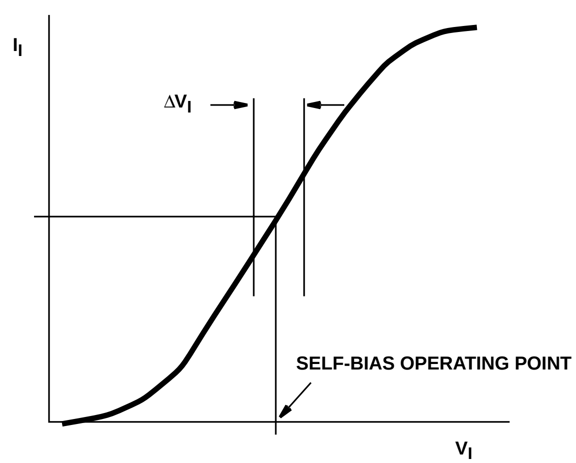


FIGURE 10. TYPICAL INPUT RESISTANCE CURVE AT SIG_{IN}, $COMP_{IN}$

Typical Performance Curves (Continued)

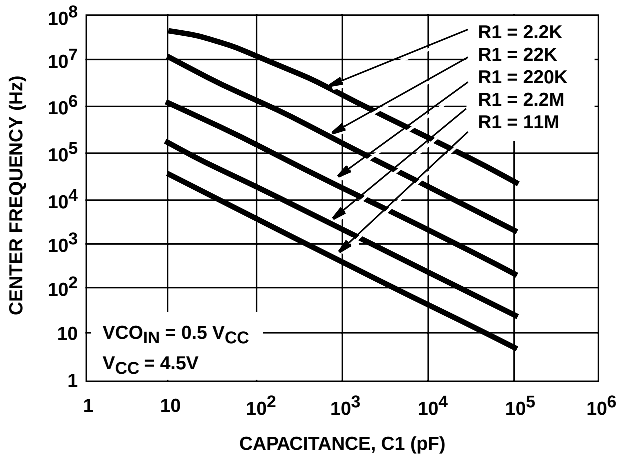


FIGURE 11. HC4046A TYPICAL CENTER FREQUENCY vs R1, C1 (V_{CC} = 4.5V)

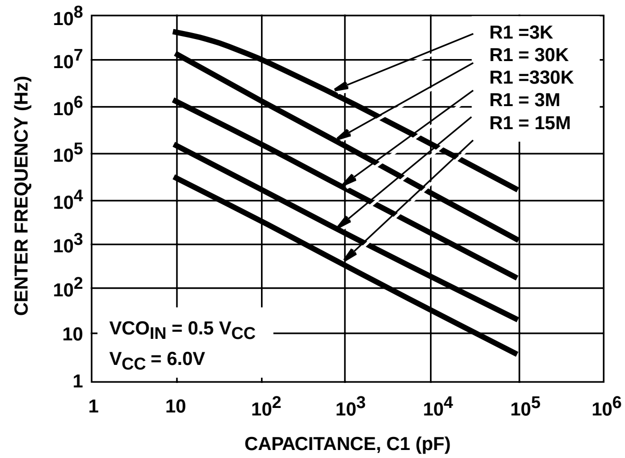


FIGURE 12. HC4046A TYPICAL CENTER FREQUENCY vs R1, C1 (V_{CC} = 6V)

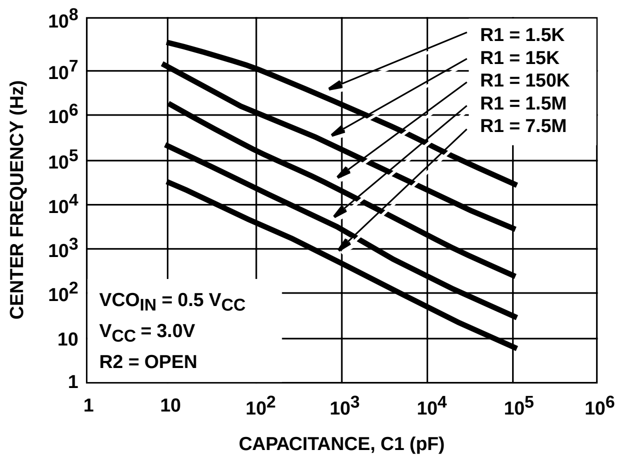


FIGURE 13. HC4046A TYPICAL CENTER FREQUENCY vs R1, C1 (V_{CC} = 3V, R2 = OPEN)

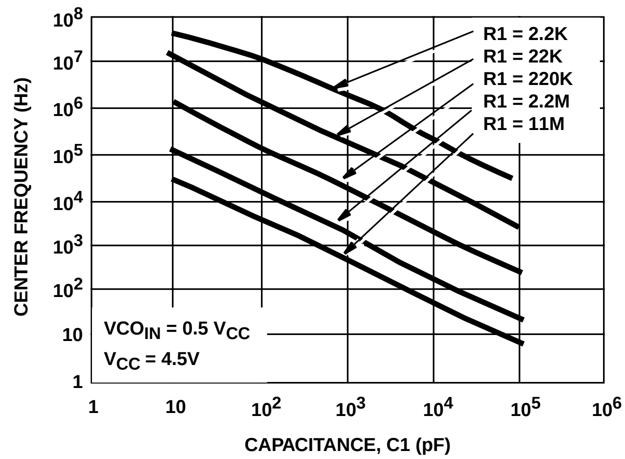


FIGURE 14. HCT4046A TYPICAL CENTER FREQUENCY vs R1, C1 (V_{CC} = 4.5V)

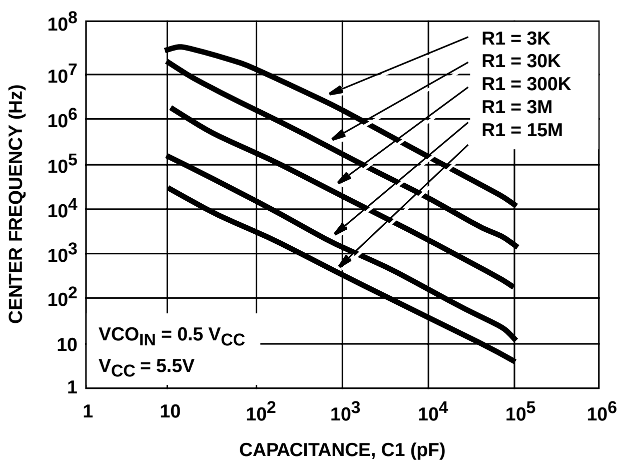


FIGURE 15. HCT4046A TYPICAL CENTER FREQUENCY vs R1, C1 (V_{CC} = 5.5V)

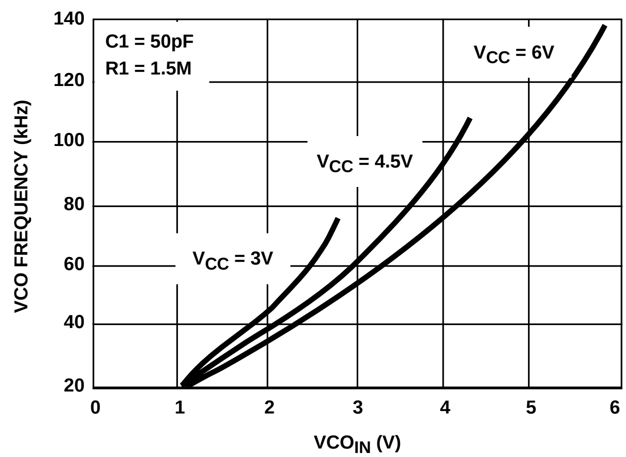


FIGURE 16. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 1.5MΩ, C1 = 50pF)

Typical Performance Curves (Continued)

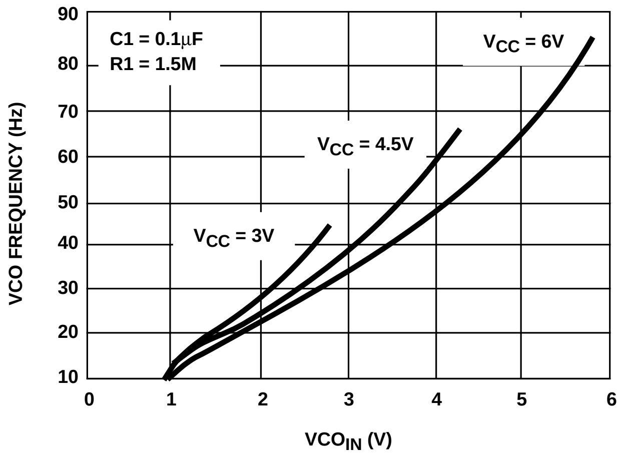


FIGURE 17. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 1.5MΩ, C1 = 0.1µF)

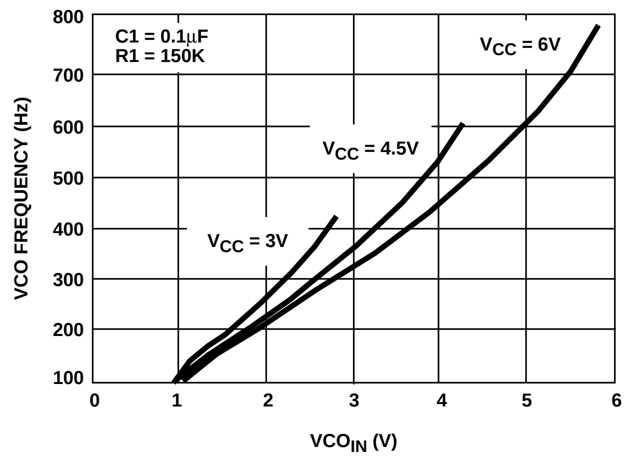


FIGURE 18. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 150kΩ, C1 = 0.1µF)

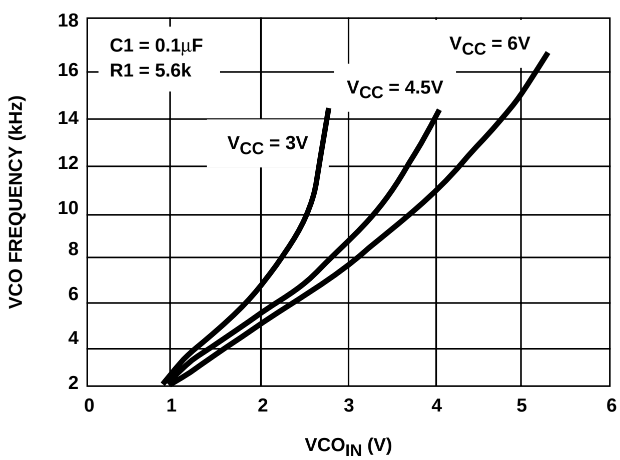


FIGURE 19. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 5.6kΩ, C1 = 0.1µF)

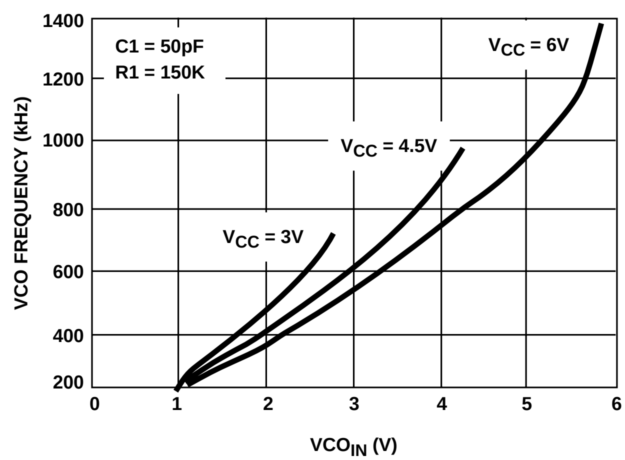


FIGURE 20. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 150kΩ, C1 = 50pF)

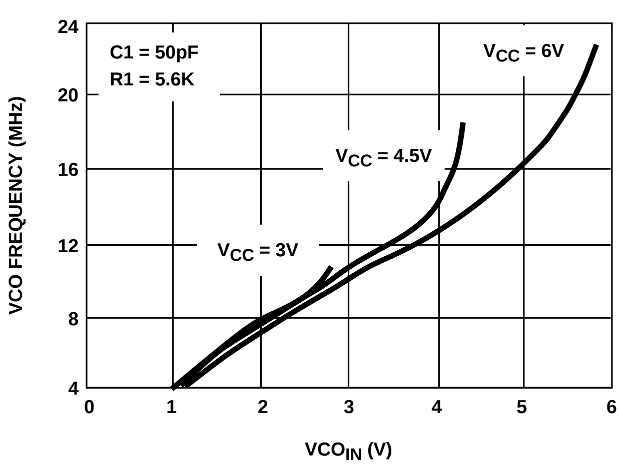


FIGURE 21. HC4046A TYPICAL VCO FREQUENCY vs VCO_{IN} (R1 = 5.6kΩ, C1 = 50pF)

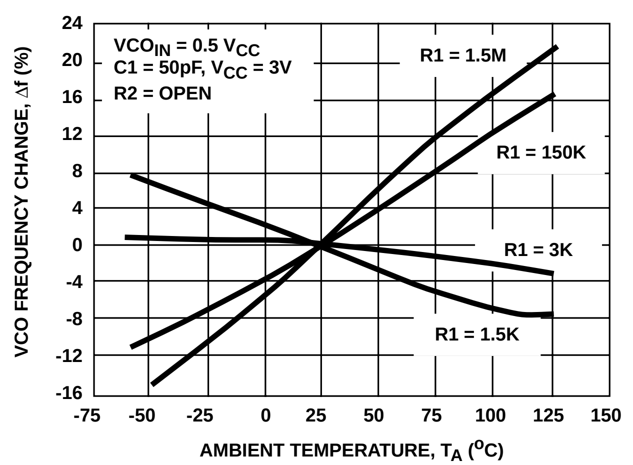


FIGURE 22. HC4046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1 (V_{CC} = 3V)

Typical Performance Curves (Continued)

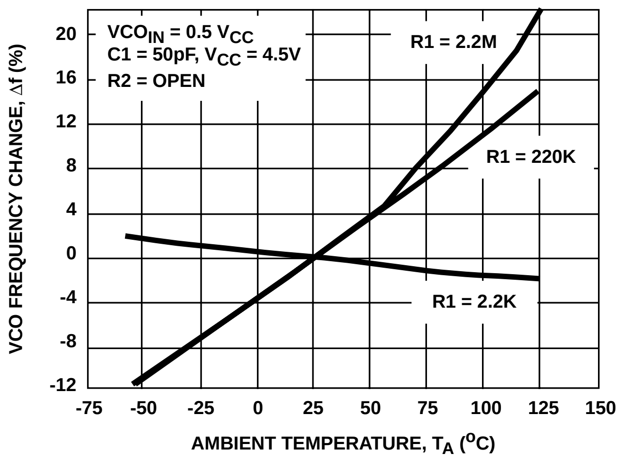


FIGURE 23. HC4046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1 (V_{CC} = 4.5V)

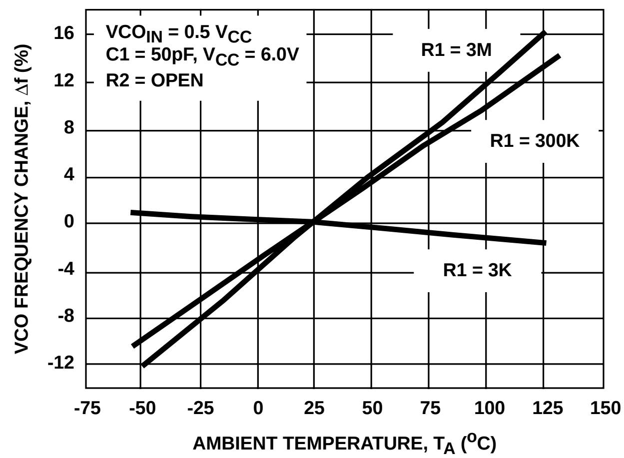


FIGURE 24. HC4046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1 (V_{CC} = 6V)

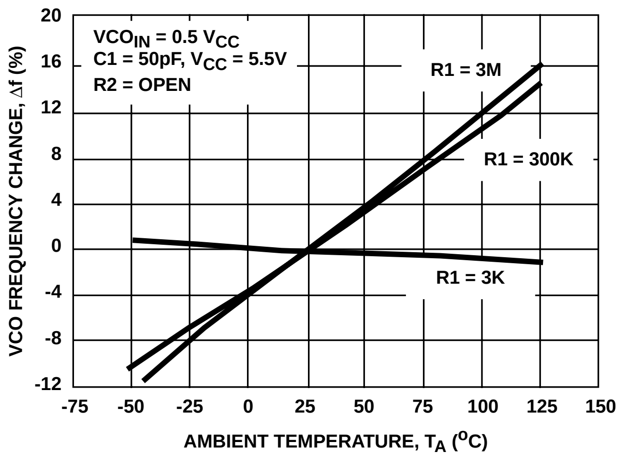


FIGURE 25. HCT4046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1

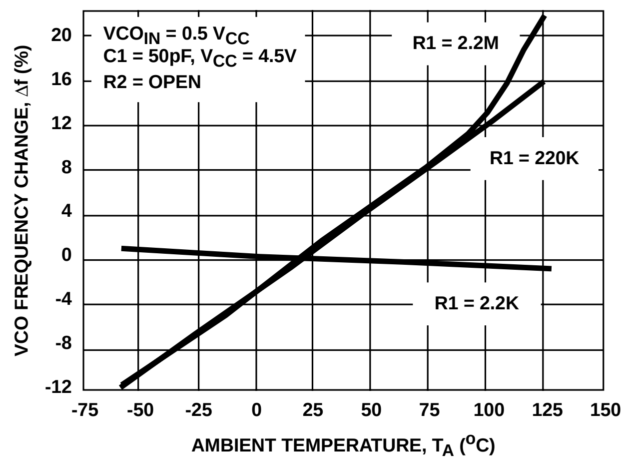


FIGURE 26. HC4046A TYPICAL CHANGE IN VCO FREQUENCY vs AMBIENT TEMPERATURE AS A FUNCTION OF R1 (V_{CC} = 4.5V)

Typical Performance Curves (Continued)

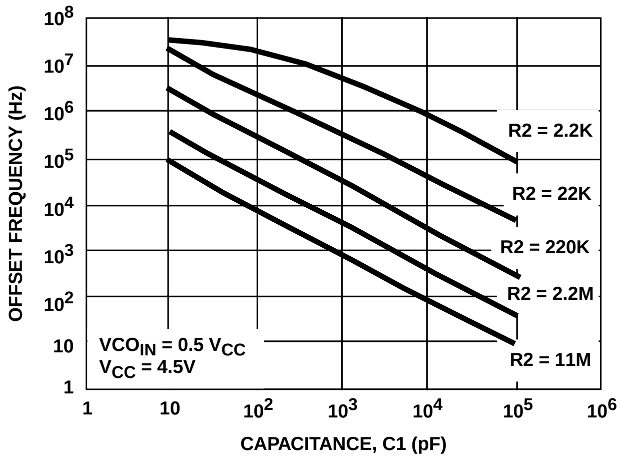


FIGURE 27. HC4046A OFFSET FREQUENCY vs R2, C1 (V_{CC} = 4.5V)

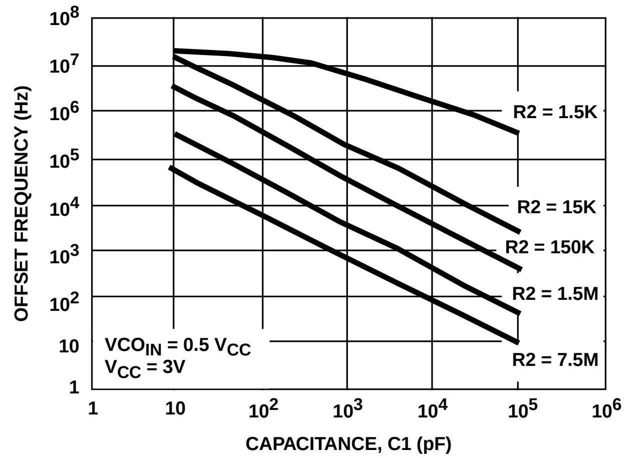


FIGURE 28. HC4046A OFFSET FREQUENCY vs R2, C1 (V_{CC} = 3V)

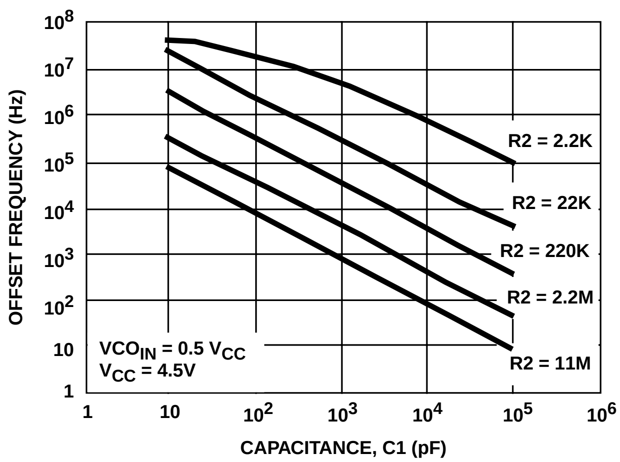


FIGURE 29. HCT4046A OFFSET FREQUENCY vs R2, C1 (V_{CC} = 4.5V)

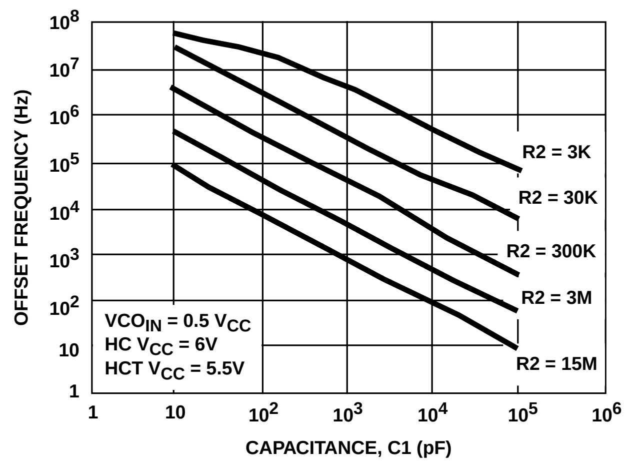


FIGURE 30. HC4046A AND HCT4046A OFFSET FREQUENCY vs R2, C1 (V_{CC} = 6V, V_{CC} = 5.5V)

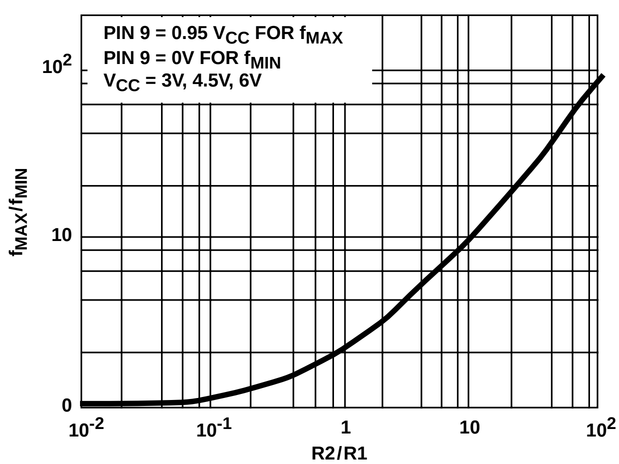


FIGURE 31. HC4046A f_{MIN}/f_{MAX} vs R2/R1 (V_{CC} = 3V, 4.5V, 6V)

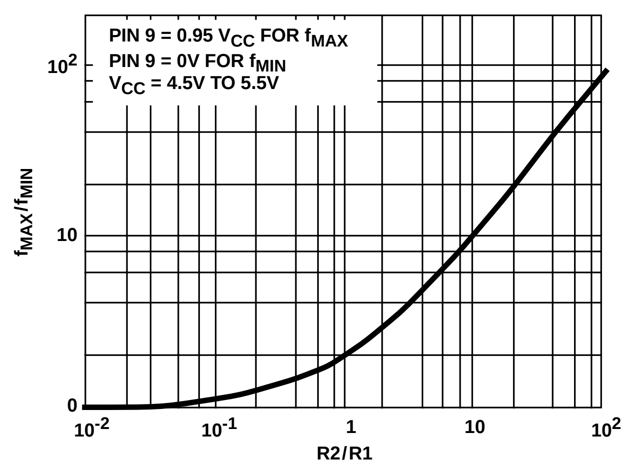


FIGURE 32. HCT4046A f_{MAX}/f_{MIN} vs R2/R1 (V_{CC} = 4.5V TO 5.5V)

Typical Performance Curves (Continued)

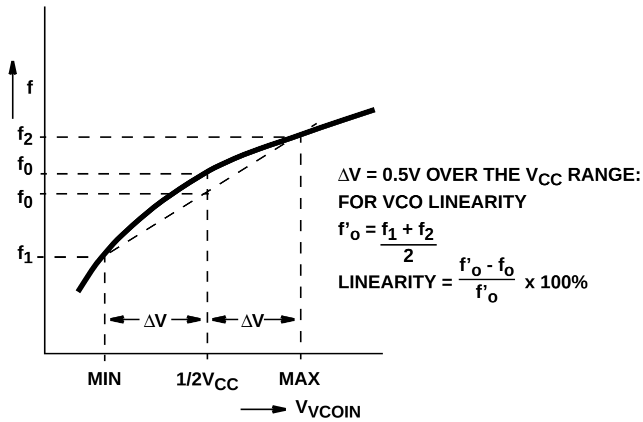


FIGURE 33. DEFINITION OF VCO FREQUENCY LINEARITY

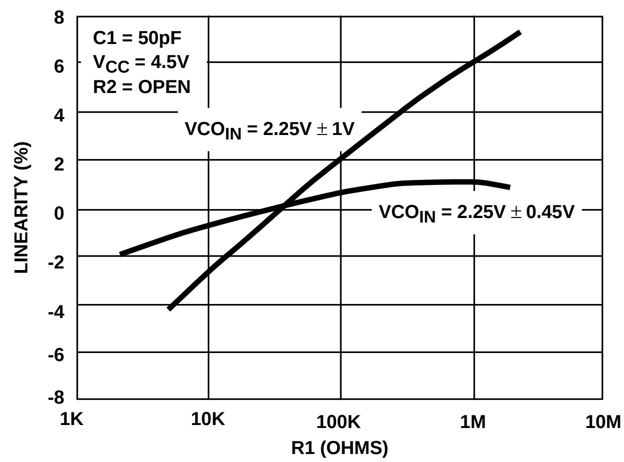


FIGURE 34. HC4046A VCO LINEARITY vs R1 (V_{CC} = 4.5V)

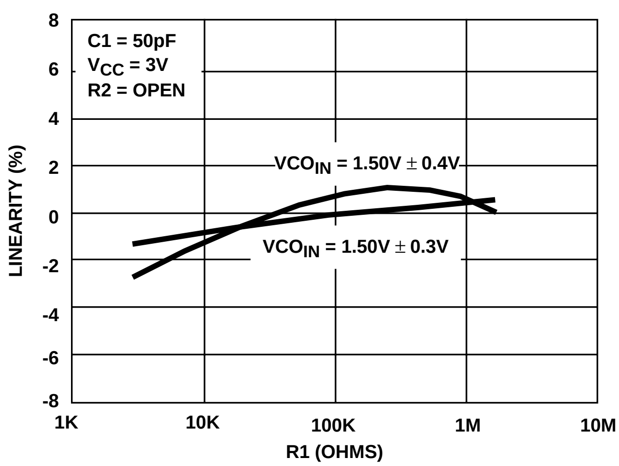


FIGURE 35. HC4046A VCO LINEARITY vs R1 (V_{CC} = 3V)

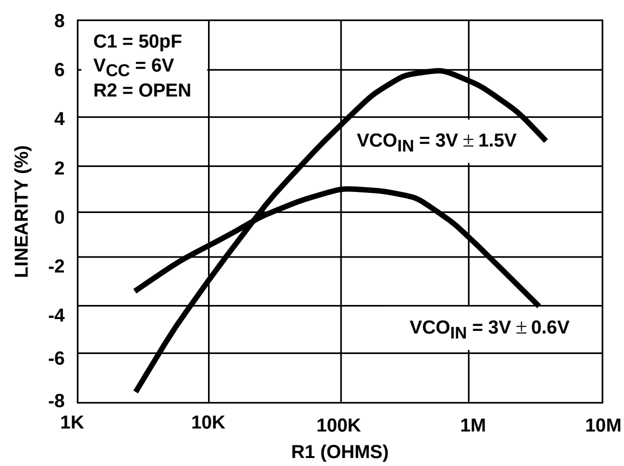


FIGURE 36. HC4046A VCO LINEARITY vs R1 (V_{CC} = 6V)

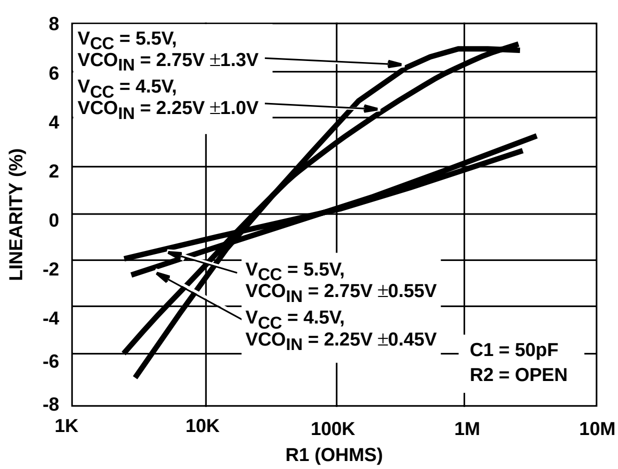


FIGURE 37. HCT4046A VCO LINEARITY vs R1 (V_{CC} = 4.5V, V_{CC} = 5.5V)

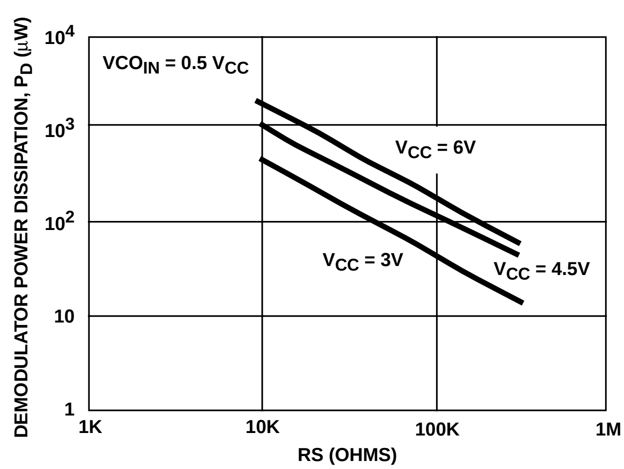


FIGURE 38. HC4046A DEMODULATOR POWER DISSIPATION vs RS (TYP) (V_{CC} = 3V, 4.5V, 6V)

Typical Performance Curves (Continued)

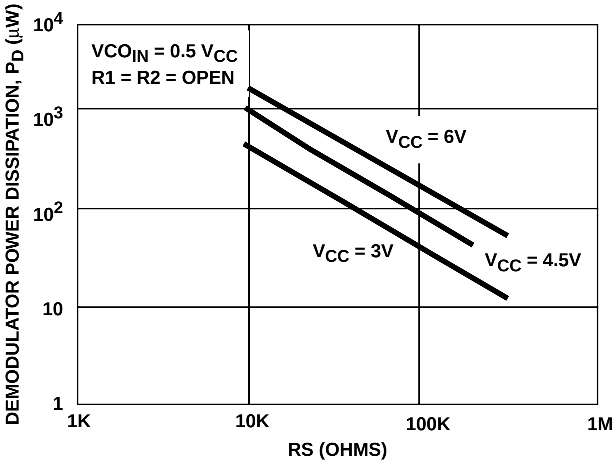


FIGURE 39. HCT4046A DEMODULATOR POWER DISSIPATION vs RS (TYP) (V_{CC} = 3V, 4.5V, 6V)

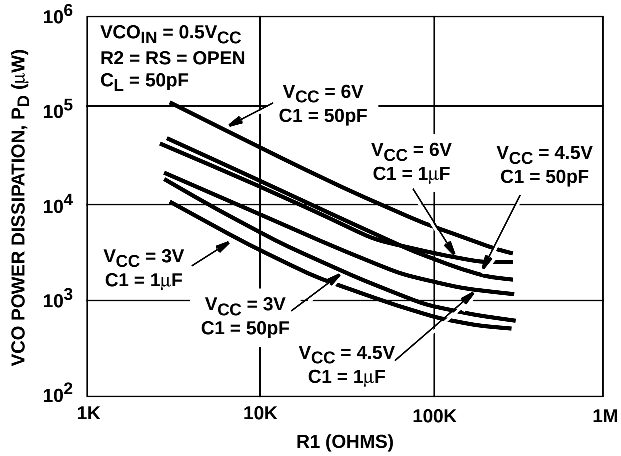


FIGURE 40. HC4046A VCO POWER DISSIPATION vs R1 (C1 = 50pF, 1μF)

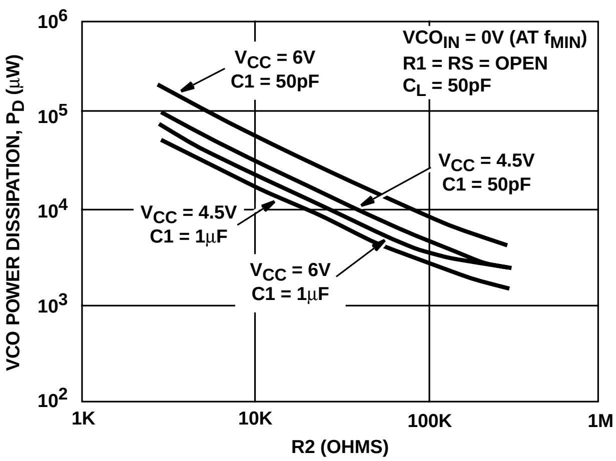


FIGURE 41. HCT4046A VCO POWER DISSIPATION vs R2 (C1 = 50pF, 1μF)

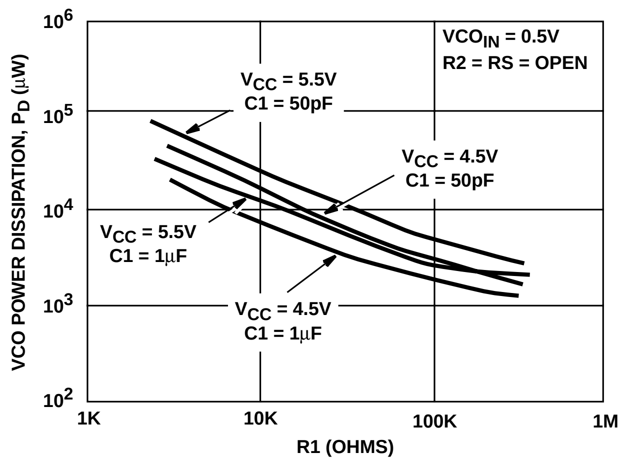


FIGURE 42. HCT4046A VCO POWER DISSIPATION vs R1 (C1 = 50pF, 1μF)

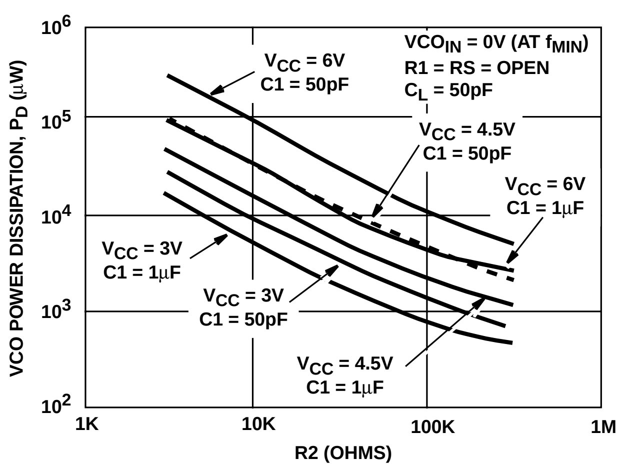


FIGURE 43. HC4046A VCO POWER DISSIPATION vs R2 (C1 = 50pF, 1μF)

HC/HCT4046A C_{PD}

CHIP SECTION	HC	HCT	UNIT
Comparator 1	48	50	pF
Comparators 2 and 3	39	48	pF
VCO	61	53	pF

Application Information

This information is a guide for the approximation of values of external components to be used with the ’HC4046A and ’HCT4046A in a phase-lock-loop system.

References should be made to Figures 11 through 15 and Figures 27 through 32 as indicated in the table.

Values of the selected components should be within the following ranges:

R1	Between 3kΩ and 300kΩ
R2	Between 3kΩ and 300kΩ
R1 + R2	Parallel Value > 2.7kΩ
C1	Greater Than 40pF

<table>
<tr><th>SUBJECT</th><th>PHASE COMPARATOR</th><th>DESIGN CONSIDERATIONS</th></tr>
<tr><td rowspan="3">VCO Frequency Without Extra Offset</td><td>PC1, PC2 or PC3</td><td>VCO Frequency Characteristic
With R2 = ∞ and R1 within the range 3kΩ < R1 < 300kΩ, the characteristics of the VCO operation will be as shown in Figures 11 - 15. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)

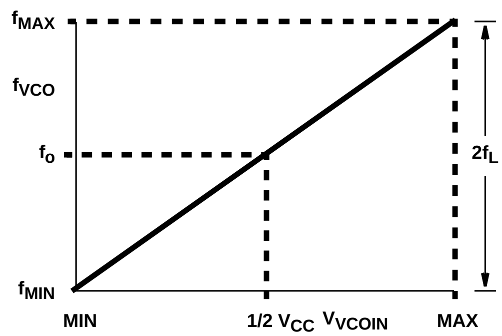


FIGURE 44. FREQUENCY CHARACTERISTIC OF VCO OPERATING WITHOUT OFFSET: f_o = CENTER FREQUENCY: $2f_L$ = FREQUENCY LOCK RANGE</td></tr>
<tr><td>PC1</td><td>Selection of R1 and C1
Given f_o, determine the values of R1 and C1 using Figures 11 - 15</td></tr>
<tr><td>PC2 or PC3</td><td>Given f_{MAX} calculate f_o as $f_{MAX}/2$ and determine the values of R1 and C1 using Figures 11 - 15. To obtain $2f_L$: $2f_L \approx 1.2 (V_{CC} - 1.8V)/(R1C1)$ where valid range of VCO_{IN} is $1.1V < VCO_{IN} < V_{CC} - 0.9V$</td></tr>
<tr><td rowspan="2">VCO Frequency with Extra Offset</td><td>PC1, PC2 or PC3</td><td>VCO Frequency Characteristic
With R1 and R2 within the ranges 3kΩ < R1 < 300kΩ, 3kΩ, < R2 < 300kΩ, the characteristics of the VCO operation will be as shown in Figures 27 - 32.

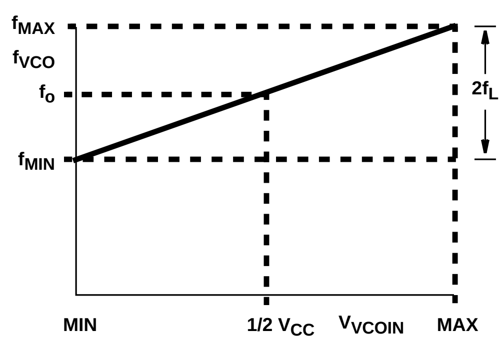
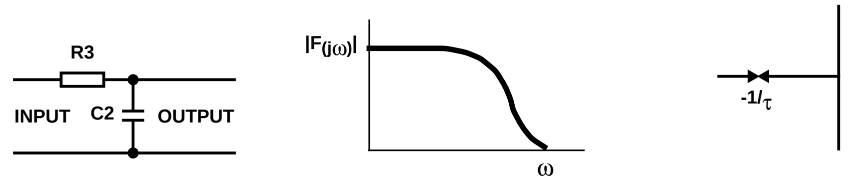
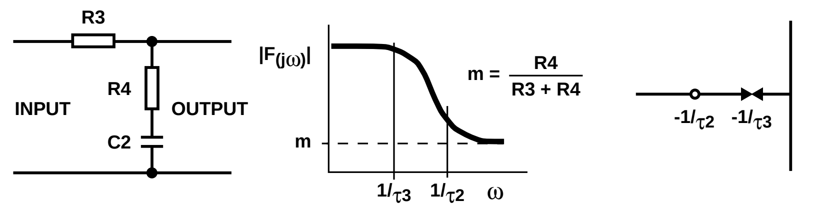


FIGURE 45. FREQUENCY CHARACTERISTIC OF VCO OPERATING WITH OFFSET: f_o = CENTER FREQUENCY: $2f_L$ = FREQUENCY LOCK RANGE</td></tr>
<tr><td>PC1, PC2 or PC3</td><td>Selection of R1, R2 and C1
Given f_o and f_L, offset frequency, f_{MIN}, may be calculated from $f_{MIN} \approx f_o - 1.6 f_L$.
Obtain the values of C1 and R2 by using Figures 27 - 30.
Calculate the values of R1 from Figures 31 - 32.</td></tr>
</table>

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL Conditions with No Signal at the SIG_{IN} Input	PC1	VCO adjusts to f_o with $\phi_{DEMOUT} = 90^o$ and $V_{VCOIN} = 1/2\ V_{CC}$ (see Figure 2)
	PC2	VCO adjusts to f_{MIN} with $\phi_{DEMOUT} = -360^o$ and V_{VCOIN} = 0V (see Figure 4)
	PC3	VCO adjusts to f_{MAX} with $\phi_{DEMOUT} = 360^o$ and $V_{VCOIN} = V_{CC}$ (see Figure 6)
PLL Frequency Capture Range	PC1, PC2 or PC3	Loop Filter Component Selection  (A) τ = R3 x C2 (B) AMPLITUDE CHARACTERISTIC (C) POLE-ZERO DIAGRAM A small capture range ($2f_c$) is obtained if $\tau > 2f_c \approx 1/\pi\ (2\pi f_L/\tau.)^{1/2}$ **FIGURE 46. SIMPLE LOOP FILTER FOR PLL WITHOUT OFFSET**
		 (A) τ1 = R3 x C2; τ2 = R4 x C2; τ3 = (R3 + R4) x C2 (B) AMPLITUDE CHARACTERISTIC (C) POLE-ZERO DIAGRAM **FIGURE 47. SIMPLE LOOP FILTER FOR PLL WITH OFFSET**
PLL Locks on Harmonics at Center Frequency	PC1 or PC3	Yes
	PC2	No
Noise Rejection at Signal Input	PC1	High
	PC2 or PC3	Low
AC Ripple Content when PLL is Locked	PC1	$f_r = 2f_i$, large ripple content at $\phi_{DEMOUT} = 90^o$
	PC2	$f_r = f_i$, small ripple content at $\phi_{DEMOUT} = 0^o$
	PC3	$f_r = fSIG_{IN}$, large ripple content at $\phi_{DEMOUT} = 180^o$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8875701EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-8960901EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4046AF	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4046AF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT4046AF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC4046AE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4046AEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4046AM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046AMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4046APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4046AE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4046AEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4046AM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4046AM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4046AM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4046AME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HCT4046AMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4046AMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

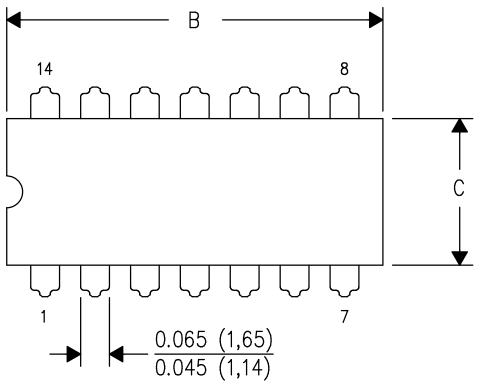
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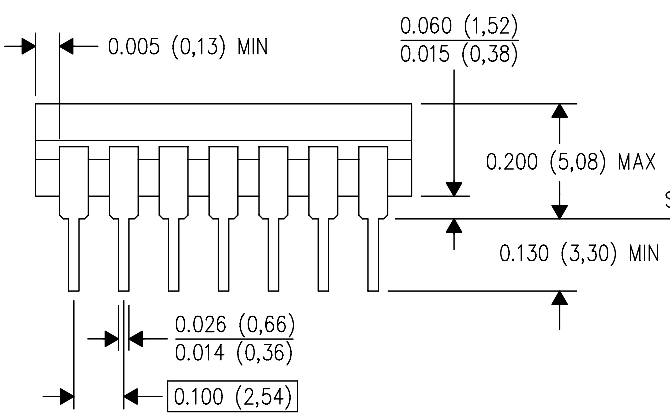
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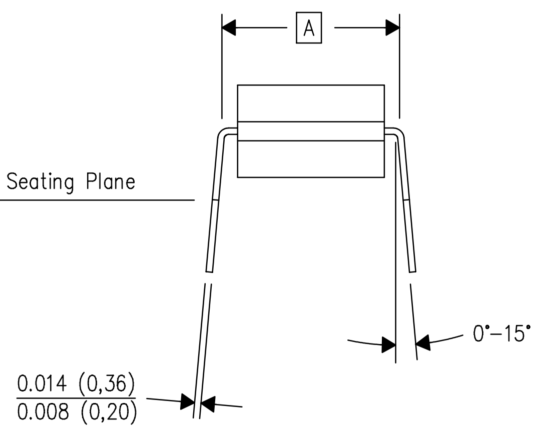
J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)







4040083/F 03/03

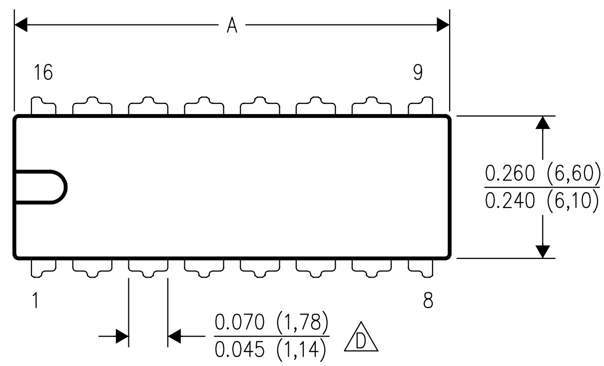
NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

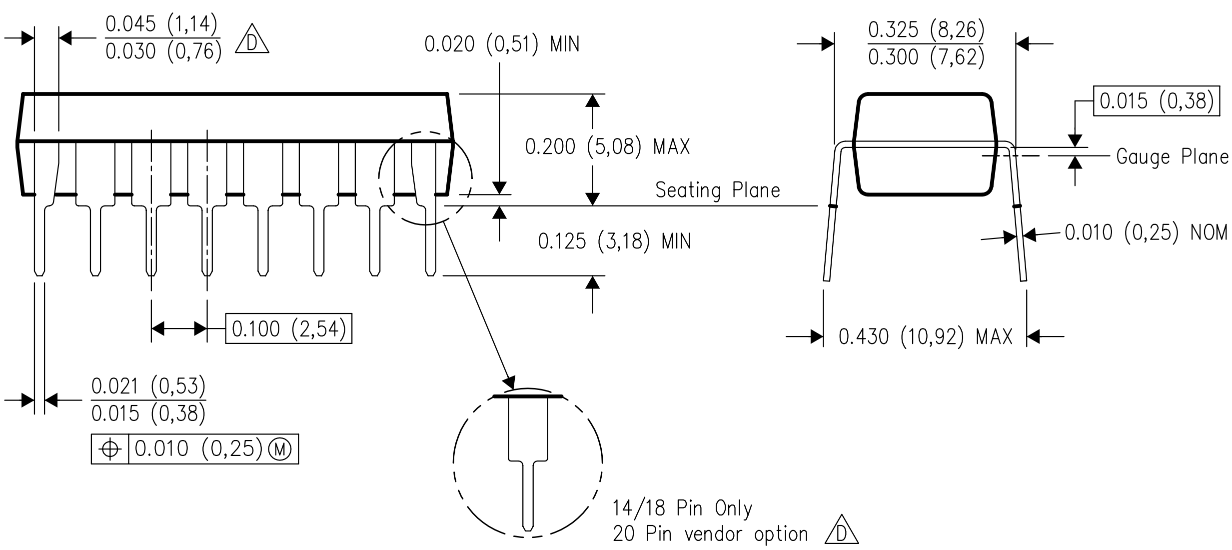
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



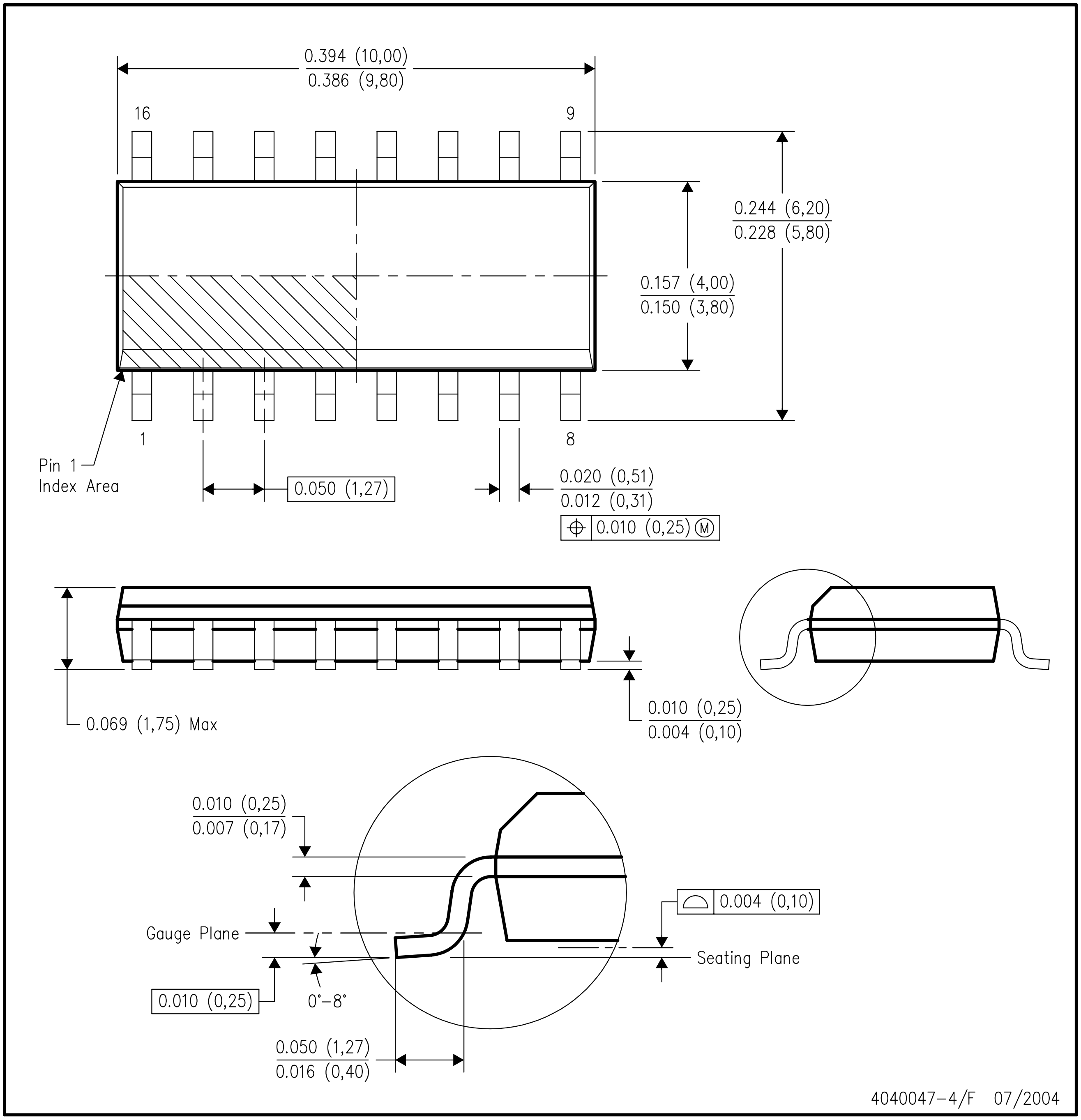
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

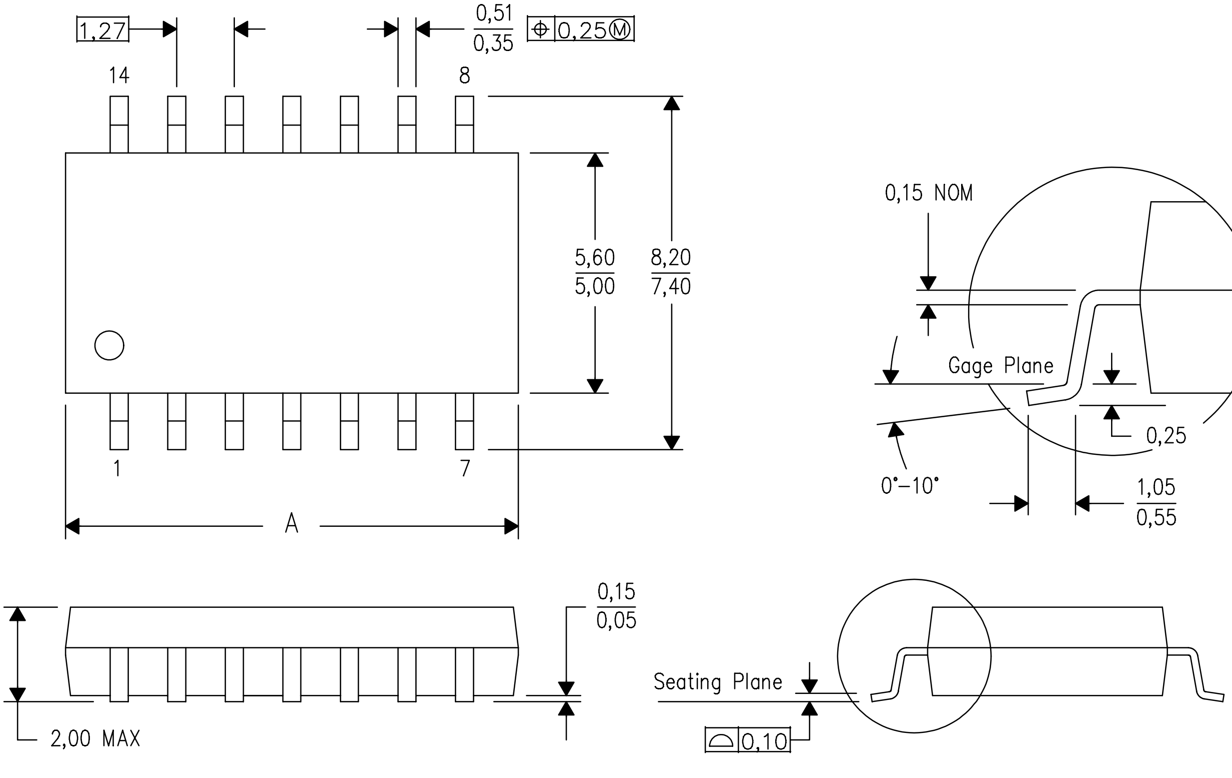
D (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012 variation AC.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



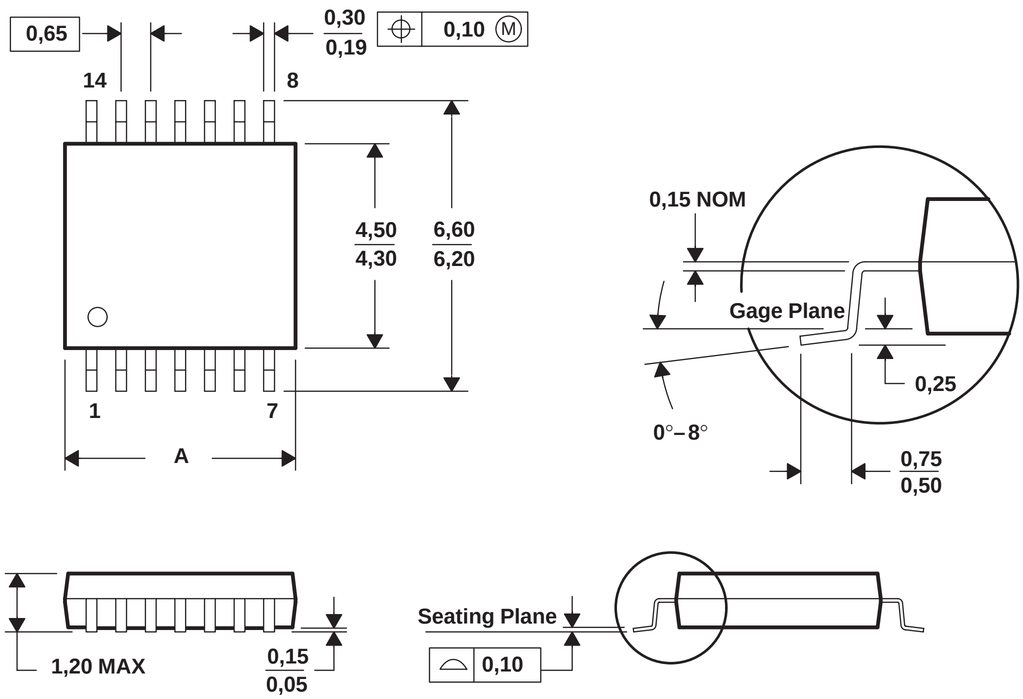
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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